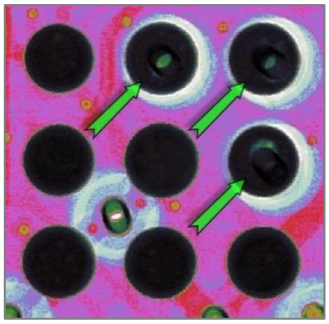
SILICON FOREST ELECTRONICS

Making a positive and profound impact.



Kev's Korner | June 2021 | Spring Cleaning

I love Spring in the Pacific Northwest and look forward to its arrival each year. As the old-timers here in SW Washington say… "Spring has sprung" when the last patch of snow has melted from the top of Silver Star Mountain (elev. 4,364'). Well, looking out the window, the snow has indeed melted on Silver Star so it's time to get outside and work in the garden, clean out the horseshoe pits, or perhaps lace up your hiking boots and head for one of your favorite trails. It is also a great time to get your Spring cleaning done, and while you're at it, why not ensure that your printed circuit board (PCB) data & documentation package is as "clean" and complete as possible, especially when it comes to vias, and even more so for filled vias.



Voiding seen during x-ray inspection as a result of unfilled vias in BGA lands.

The words "filled vias" never fail to remind me of other amusing oxymorons, such as "jumbo shrimp", "accurate estimate", "working vacation", and my all-time favorite, "cleaning no-clean" 😉. Filled vias are a true contradiction in terms ~ Why would you drill a hole in a PCB and then turn around and fill it back up? Well, as my colleague explained in a previous article (May 2019, Mama Via! It's a Via!), there are many good reasons for having specific sized vias filled on your PCB. For example, when your design includes a footprint that does not allow room for standard trace routing, such as for a fine-pitch BGA, via-in-pad becomes the only option. That's great, however there are now a bunch of inconvenient holes drilled through the center of the surface mount lands of this BGA footprint that we eventually need to solder. Because of this, these vias need to be filled and overplated (often referred to as "VIPPO" ~ via-in-pad-plated-over), during PCB fabrication in order to prevent potential solder joint defects such as voiding and insufficient solder during assembly.

Since there are often many different sizes of vias (as well as other holes) on the PCB, it is important to be very clear on exactly which size vias require filling (and which sizes do not). We see many good examples of this and wanted to share a few of them with you in case you would like to use one or all of them in your documentation (see below). Probably the simplest is to include a note on your PCB fabrication drawing indicating which via sizes require filling. In addition, adding a "FILLED" column to your drill chart is another great way to identify specific drill sizes that require filling. Finally, adding a "layer" to your PCB data that includes the drills that need to be filled is also very helpful and serves as a great visual indicator when viewing the design data. Since we are the classic "belt-and-suspenders" types around here we recommend using all three.

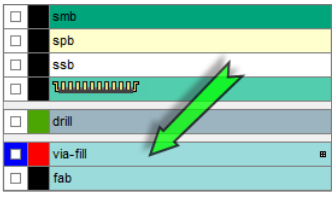
17. VIA FILL: ALL 10.0 AND 15.0 MIL VIAS SHALL BE FILLED WITH NON-CONDUCTIVE EPOXY AND PLATED-OVER (IPC-4761 TYPE VII).

Via fill note on PCB fabrication drawing.

DRILL CHART - ALL SIZES IN MILS

QTY	SYM	SIZE	TOL	LAYERS	PLATED	FILLED
527	+	10.0	±3	1-8	YES	YES
200	⊠	15.0	±3	1-8	YES	YES
413	◇	25.0	±3	1-8	YES	NO
5	□	125.0	±5	1-8	NO	NO

Via fill column on PCB fabrication drawing.



Via fill layer in PCB design data.

As always, if you have any questions or comments, please feel free to reach out to us here at SFE.

Thanks for reading!

Contributed by:
Kevin Syverson | Chief Technical Officer | Silicon Forest Electronics | kevin@si-forest.com