SILICON FOREST ELECTRONICS

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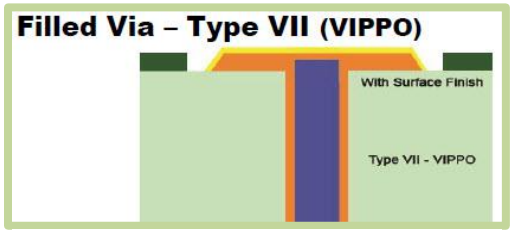
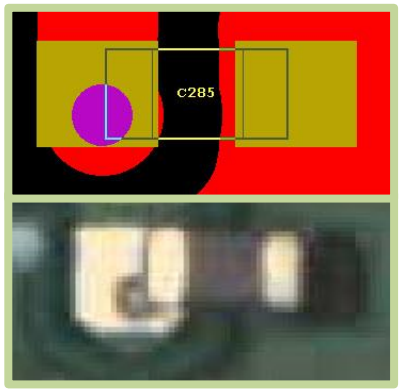
Process Engineering Notebook | May 2019 | Mama Mia! It's a Via!

One of the most important parts of a Printed Circuit Board Assembly (PCBA) may also be the leading cause of defects from a Design for Manufacturability (DFM) standpoint: vias. For the uninitiated, a via is small hole plated with copper that electrically connects different layers of a multilayer Printed Circuit Board (PCB). PCBs can have thousands of vias depending on size and complexity, so as you can imagine that leaves a lot of opportunities for potential issues. In all of the DFM reviews I have performed, issues relating to vias have undeniably taken the cake as the most common. My carpal tunnel may start acting up if I try to address even just a fraction of the issues vias can cause, so for this article I will focus on vias in or near Surface Mount Technology (SMT) lands.

The first culprit of defects is the infamous via-in-pad. Via-in-pad is a very useful tool, whether it's for routing of a fine pitch BGA component or simply saving space in a high density design. However, if not done correctly it can lead to extensive rework which, especially in the case of a BGA, can be expensive. The remedy for via-in-pad is quite simple; specify fill and overplate for vias-in-pad on the fabrication drawing, often referred to as VIPPO (via-in-pad plated over). This will prevent solder from flowing down the via during reflow, which may lead to solder joint defects. This option does add extra cost to PCB fabrication, however the amount saved on potential rework makes this a small price to pay. Now you might be thinking, "Colin, why can't I just fill the via with no overplating to save on cost?" True, this will prevent solder from wicking down into the via but it introduces a new variable into the equation. You have now created a land for your component that has a different solderable surface area than its adjacent lands, which can lead to a number of issues. Now, if you are specifying a HASL (hot air solder leveling) finish on your PCB everything changes. This surface finish will fill exposed vias during the fabrication process, which is great news! However, a HASL finish is not the best choice for PCBAs with fine pitch assembly (0.020" and below), fine-feature lands, or any BGA component due to its poor planarity.

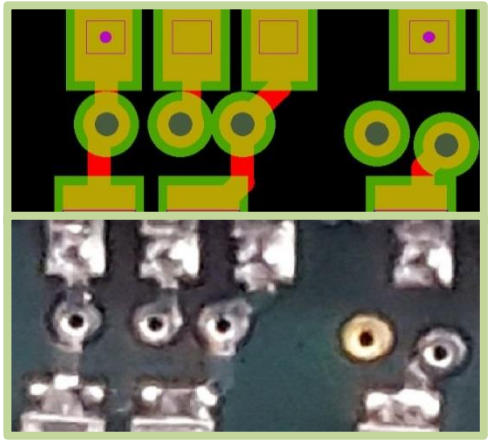


VIPPO Option: Image provided by our friends at Westak.



Via-in-pad starving the solder joint of a passive component. (Top image: Design Data, Bottom Image: PCBA Image)

My great Italian grandmother used to have a saying: "keep your friends close, and your vias closer." Too bad she was wrong. Our second issue revolves around the minimum spacing between vias and component lands and the use of soldermask dams. Often we see an attempt (or no attempt at all) at creating a soldermask dam between component lands and exposed vias and as is the case with dams in general, bigger is always better. A small soldermask dam may break away during fabrication which, like any dam break, may result in a flood of



Missing soldermask dams causing solder to wick down exposed vias. (Top image: Design Data, Bottom Image: PCBA Image)

Soldermask clearance connecting a via to a component land, resulting in a tombstone defect.

solder where you don't necessarily want it. Depending on their capabilities and material offerings, most PCB fabricators can typically achieve minimum soldermask dams of 0.002" for LDI (Laser Direct Imaging) and 0.003"-0.004" for LPI (Liquid Photo-Imageable). If a via needs to be exposed for testing purposes, the simple fix is to increase the space between the via and land to allow for a proper soldermask dam. If the via doesn't need to be exposed the alternative option is to cover it with soldermask, often referred to as a tented via. For this process it is best to only cover the via with soldermask on one side of the PCB. If both sides are covered, contaminants trapped during PCB fabrication may volatilize during thermal processes resulting in potential defects during assembly. If tenting on both sides is required, the best recommendation would be to fill the via. This will prevent anything from becoming entrapped inside. Another potential issue to be aware of, if deciding to cover the via with soldermask, is the registration tolerance. Typical LPI soldermask registration tolerance is 0.002" to 0.004". This means that even if a via is covered with soldermask, if it's within the registration tolerance from the land it could become exposed allowing solder to wick down inside. If you have a high density design where these spacing and tolerances can't be met, it may be best to use via-in-pad.

If you have made this far without dozing off, I congratulate you and hope that you have gained some useful knowledge on via design for manufacturing. We look forward to working with our customers on best practices for not only vias but for all of the various features on the PCBA. As always, please don't hesitate to contact us for any questions, comments or further information.

Thanks for reading!

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