



plug & play instruments
oscilloscopes

Phone +64 9 524 7456
Email support@cleverscope.com
Web www.cleverscope.com
21A Lancing Rd, Sandringham
P.O. Box 26-527
Auckland 1025
New Zealand

12 July 2018 v1.2

CS448 Isolated Channel Oscilloscope Specification

Summary

The CS448 is an individually isolated channel high CMRR oscilloscope with four channels. It is designed to measure all the signals in an operating full or three phase power electronic switching bridge. Examples include gate drives to measure voltage and charge, the power switch to measure loss and parasitic stress, the output to measure power and spectrum for EMC compliance, and the control system for Gain/Phase and stability. The CS448 includes an isolated signal generator for stimulus, and eight digital inputs to measure control signals. Two CS448's can be slaved to make an 8 channel oscilloscope with coherent sampling. See the selected measurements at the end of the specification section for visual examples of measurements made.

Front



Chan A - Chan D inputs:

- 1kV operating isolation voltage to ground and other channels.
- Withstands 1kV input voltage
- 100 dB CMRR at 50 MHz
- 14 bit resolution, 100dB dynamic range
- 200 MHz BW
- 14 pF to chassis
- 100uV resolution on 0.8v range
- 200uV rms noise on 0.8V range
- probe isolators for protection.

IN 1-8 Digital inputs:

- Isolated 1kV working (2 separate pods of 4 channels with a common)
- 400 Mbps
- 5 pF to chassis
- 100 kV/us transient immunity
- Logic level threshold voltage.

Back



Signal Generator:

- Isolated 600V working
- 0 - 65 MHz
- 14 pF to chassis
- 100 dB CMRR at 50 MHz
- Sine, arbitrary (incl patterns). 100uV rms noise

Digital Port:

- 16 bi-directional pins connected to Silego SLG46533V analog/digital programmable device
- Trigger In/Out connection

Link Port:

- Links to CS1070 0-50 MHz 1A power amplifier, CS1110 VCE Sat probe.
- Includes Uart, SPI and I2C I/O
- Trigger and control

SD Card:

- Store stand-alone captures to the SD Card

USB:

- USB 3-C socket
- USB3 @ 200MBps
- USB2 @ 30 MBps

Ethernet:

- SFP socket based
- Copper 10/100/ 1000 Mbps
- Fibre 1Gbps

Link In/Out:

- Used to daisy chain multiple units
- Synchronous sample clock
- Trigger and control

Power In:

- 10- 24V DC, 36W.
- Can be car power supply connected, withstands crank and load dump.

Triggering

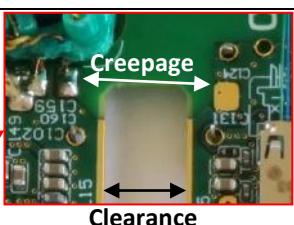
- Two FPGA mixed signal triggers
- Triggers interpolate in time for higher trigger accuracy.
- Triggers may be combined using AND/OR/XOR
- Triggers may be sequences Trigger 1 [num occurrences] - time specification - Trigger 2 [num occurrences] . The time specification is less than a period, in a period range or more than a period. Triggers may be completely independent.
- The digital portion may be rising or falling digital input, conditional on one or more other digital inputs being 0, 1 or don't care. Bit's may be OR'd or AND'd.
- The analog trigger may be conditional on a digital state.

Analog Inputs

* Item still to be implemented. See Specification Status section.

Parameter	Specification	Notes
Number of channels	4	Fibre optic isolated from each other
Isolation Voltage	1kV working Cat III, when connected to mains systems of less than 300V line-neutral	Supported by IEC 61010-1 Ed 3.0 and IEC 61010-2-30 (Test Equipment) creepage and clearance, reinforced, Category III Plan to certify
CMRR	> 120 dB at 1 MHz > 115 dB at 10 MHz > 100 dB at 50 MHz	Done using a 20 dBV test source
ADC resolution	14 bits	
Input Ranges	$\pm 0.8V$ and $\pm 8V$	Use probes to extend the range, eg 800V with 100x probe. The application automatically scales all values to compensate for probe attenuation.
Sample Rate	500 MSPS * 400 MSPS now	All Analog and Digital channels simultaneously.
Sample Memory	250 M Samples *	Currently 4 x simultaneous channels with 10M per channel.
CM leakage to other channels	<-125dBc	20 dBV signal to CM channel, measured on other channels whole bandwidth, $\pm 0.8V$ range
Channel to Channel Skew	< ± 144 ps	Done using a 1 MHz coherent sine wave
Cross talk at 10.7 and 30 MHz	< -115 dBc	Using 1.6V p-p into the channel
RMS Channel Noise 1 M samples	< 200 uV rms, $\pm 0.8V$ range < 2mV rms, $\pm 8V$ range	Inputs open
Pk-Pk Channel noise 1 M samples	1.8mVp-p for $\pm 0.8V$ range 15mVp-p for $\pm 8V$ range	Inputs open
Sample clock jitter	300 fs rms	
Sample clock Freq tolerance	± 10 ppm	At 23 deg C
Sample clock temp stability	± 15 ppm	Over -40 to +85 deg C
Enob (rms)	11.6 bits, or 1 part in 3,300	Inputs open
Noise free bits	10.3 bits, or 1 part in 1300	Inputs open
Spectral Noise floor, no protrusions	-100 dBV -115dBV	<2MHz, 200 MHz BW, 1kHz resolution >2MHz, 200 MHz BW, 1kHz resolution
Sinad	> 64 dBc at 1 MHz > 63 dBc at 10 MHz > 55 dBc at 30 MHz	1 Vp-p into 50 ohms signal
HD2+3	< -80dB at 1MHz < -76 dB at 10 MHz < -71 dB at 30 MHz	1 Vp-p into 50 ohms signal
THD	< -76 dB at 1 MHz < -74 dB at 10 MHz < -67 dB at 30 MHz	1 Vp-p into 50 ohms signal
Pulse Flatness	< 700uV < 2mV < 200mV	0.5V pulse, 500us duration, $\pm 0.8V$ range 0.5V pulse, 500 us duration, $\pm 8V$ range 500V pulse, 500us duration, 100x probe
Overload recovery	4ns	Recovery from 10x overload
Maximum Differential Input Voltage	± 1 kV, derated above 1 MHz.	Derated at 20dB/decade
Maximum Common Mode Input Voltage	± 1 kV, derated above 10 MHz.	Derated at 20dB/decade
Spectral Flatness	± 0.2 dB from 0 - 160 MHz -2 dB at 200 MHz	Supports 200 MHz Bandwidth
Input Resistance	1 M Ohm	DC resistance
Input Capacitance	20 pF	Signal Input to Signal Common
Isolation Capacitance	< 14pf	Channel ground to chassis

Channel to Channel Isolation

Parameter	Specification	Notes
Digitizer Board	 Minimum PCB creepage = 11 mm Minimum Clearance = 6.6 mm	IEC61010-2-030 Ed 1.0 (Test Equipment), Table K.13. 1000VAC, requires >10mm for reinforced, Materials group 1, II, III, pollution degree 2 IEC61010-2-030 Ed 1.0 (Test Equipment), Table K.101. 1000V, Measurement Category III, mains circuits up to 300V line to neutral requires >5.9 mm reinforced.

Digital Inputs

Parameter	Specification	Notes
Number of inputs	8	
Common mode transient immunity	100 kV/us	
Input threshold max	2.3V rising 0.9V falling	Using CS1006/7 isolated probes (ISO7844). Using CS1004/5 probes, threshold programmable 0-8V.
Isolation capacitance	< 5pF	To chassis ground, at 1 MHz
Isolation operating voltage	880V DC 1130V DC	Re-inforced insulation, EN61010-1 Re-inforced insulation, CSA and IEC 60950-1
Maximum Data rate	100 Mbps	Sampled at 500 MSPS* (400 MSPS now).
Propagation delay	13ns typ	Compensated for within CS448

Signal Generator

Parameter	Specification	Notes
Output Frequency Range	DC - 65 MHz	-3dB at 65MHz on un filtered output
Outputs	Unfiltered, filtered	Unfiltered is used for Frequency Response Analysis and has maximum flatness. Filtered output includes reconstruction filter for maximum smoothness
CMRR	> 120 dB at 1 MHz > 115 dB at 10 MHz > 100 dB at 50 MHz	Limited by analog inputs used for test. 20dBV signal applied to coax common linking sig gen and analog input.
Common mode transient immunity	100 kV/us	For control of the output DAC
Isolation Voltage	800VRMS working	Supported by IEC 61010-1 creepage and clearance, reinforced, Category III Plan to certify
Unfiltered rise/fall time	3.2ns	Full scale swing
Sine Wave Flatness	±0.2 dB +0.2 -3 dB	0 - 30 MHz filtered + unfiltered 30 - 65 MHz unfiltered
DAC resolution	14 bits	
NCO Resolution	24 bits	10.7 Hz resolution at 180 MSPS
Output amplitude	±1mV to ±3.5V p-p	Programmable 1mV resolution, constrained to total range ±3.5V including offset
Output offset	0 to ±3.5V p-p	Programmable, 1mV resolution
Output Noise	< 100uV rms	
SFDR	> 84 dBc	At 10 MHz
IMD	> 88 dBc	At 10 MHz
HD2+3	< -77dBc	At 10 MHz
Arb Waveform Memory	4 k Samples *	Using AD9102 - UI to be implemented still
Sample Rate	180 Msps	Programmable Sample rate 1sps - 180 Msps
Frequency list values	2k *	Frequency list output in response to trigger
Envelope can be amplitude modulated	Yes *	
Pattern Generator	Yes *	Start period, output period, stop period, pattern repeat count.
Trigger	Input from FPGA *	FPGA may trigger a pattern based on Channel Trigger or other event.

USB

Parameter	Specification	Notes
Supported Modes	USB 2.0 and USB 3.0	USB 2.0 @480 Mbit/sec and USB 3.0 at 5 Gbps
Throughput	30 MBps and 180 MBps	
Connector	USB-C	Plug is reversible
Protection	Common mode choke + ESD diodes	Using ECMF04-4HSWM10
Indicators	USB on and correctly connected	Loss of signal is indicated by LED off.

Ethernet *

Parameter	Specification	Notes
Connection method	Small Form factor Pluggable module (SFP)	An SFP socket is provided for use with an SFP module. Either an optical or a copper connected SFP module will be supplied based on the order.
Wired Supported Modes	Ethernet 10/100/1000 *	Using an RJ45 Ethernet socket connected copper SFP module. Transformer based isolation. 
		Software being implemented
Optical supported mode	Ethernet 1000BASE-LX *	Gigabit (1G) Ethernet using an LC fibre cable connected optical module. Full optical isolation. 
		Software being implemented
Throughput	12 MBps and 120 MBps	
Connector	SFP Socket	Small Form Factor Pluggable socket
Indicators	Ethernet on and correctly connected	Loss of signal is indicated by LED off.

Power Supply

Parameter	Specification	Notes
Input Voltage Range	10-24 DC	
Power consumption	36W	
Connector	Barrel Socket, 2.5mm I.D. x 5.5mm O.D	Connection is reverse polarity protected.
Protection	Clamped to +68V Clamped to -32V Operates with 35V Survives with 5V	ISO16750 pulse A (79 ohm 0.5 ohm) ISO7637 Pulse 1 (-600V, 50 ohm) FPGA operation at 5V, ADC operational at 7V.
Indicators	Power On	Software controlled.

Digital Port *

The Digital Port is based on a programmable logic IC, and can be used for generating complex state based sequences or reacting to a complex set of inputs. The port includes triggering capability. The UI has not been completed.

Parameter	Specification	Notes
Input/Outputs	16	Programmable as In or Out
Logic Level	Programmable 1.8 - 5V	All I/O operate at the same logic level
Control IC	Silego SLG46533V	User configurable programmable logic with analog functions
Resources	24 Look Up Tables (LUTs) Prog Oscillator, 25MHz, 2MHz, and 25 kHz. Prog Delay, 3 Output 16x8 RAM and OTP 4 Analog Comparators 2 x Deglitch filters	2-4 bit for complex logic All resources can be arbitrarily connected as required.
Programming	Silego GP Designer	Visual schematic designer of circuit functions downloaded into CS448
Trigger In/Out	Bidirectional Trigger	The trigger may be programmed to initiate a Digital Port sequence, or the Digital Port can trigger an analog acquisition.
Protection		Over voltage protection to +12V and -6V

Link Port *

The Link Port is used for controlling Cleverscope accessory devices such as the CS1070 1A 50 MHz power amplifier, and the CS1110 V_{CE} Sat Probe. It also includes RS232, SPI and I²C ports for controlling user equipment.

Parameter	Specification	Notes
Digital Port Use	2 Digital In, 4 Digital Out	Used for accessory control
I ² C Port	400 pbps port	For control of user devices
SPI Port	1 MHz SPI Port	For control of user device, mutually exclusive with RS232 Port
RS232/RS422 Port	3V level RS232 port, or differential RS422 port, programmable baud rate	For control of user device, mutually exclusive with SPI Port
Trigger Port	Trigger In/Out and control	Used for linkage to CS328A link port
Protection		Over voltage and reverse voltage protection using ESD devices

Link In/Out Port*

The Link In/Out Port is used daisy chaining 2 or more CS448 Cleverscopes.

Parameter	Specification	Notes
Clock ports	Reference clock, 500 kHz	The last CS448 in the chain provides the 500 kHz reference clock that is used for simultaneous sampling by all units.
Trigger Ports	Trigger transfer	The Trigger Ports transfer the triggering unit's trigger to other units.
Control Ports	Control signals	The control signals are used to signal readiness to trigger, and sampling state.

Probe Compensator Output

The probe Compensator output is used to compensate the probe response for time domain flatness.

Parameter	Specification	Notes
Signal	1 kHz Square Wave	
Amplitude	2V	Output impedance is 1.3 kOhm.
Rise Time	250ns	Limits EMC and overshoot issues

Environmental

Parameter	Specification	Notes
Temperature	0°C to +40°C -20°C to +60°C	Operating Storage
Cooling Method	Fan Assisted	
Humidity	0°C to +40°C >40°C	<90% relative humidity <60% relative humidity
Altitude	<3,000m 15,000m	Operating Non-operating

Mechanical

Parameter	Specification	Notes
Size	Height 55 mm Width 164 mm Length 247 mm	Including feet Including connectors
Weight (approx)	1150 gm 2400 gm	Acquisition Unit only Complete in display box
Material	Powder Coated Aluminium	

Specification Status

The CS448 is FPGA based, and upgradeable in the field. The customer can use Cleverscope Rom Loader tool to download new firmware and logicware to improve or add functions to the unit. The hardware system for the CS448 has been thoroughly tested to meet the specifications above, and includes all the resources needed to meet the full specification. However some software functions are still to be added. As these are added, updates are placed on our website for download at no cost. Cleverscope has used this method for years to add features such as FRA, streaming, complex maths etc. Should the current specification set meet your needs, you are able to use the CS448 now, and upgrade, at no cost, as further functionality becomes available.

Key features that still have to be implemented are:

Feature	Specification	Note
Sampling Rate	500 MSPS	Currently the sample rate is 400 MSPS. It will be upgraded to 500 MSPS on the completion of the Ethernet system.
I/O Interfaces	Ethernet is supported	Ethernet is currently not supported. We have implemented a hardware based IP stack, which is functional. Integration is proceeding with the CS448 firmware. We expect this to be complete in Aug 2018.
Sample Memory	250 MSamples.	Physical memory for 250 MSamples (16 bit) is provided. Currently we use only 40 MSamples of it organized as 4 fixed simultaneous buffers of 10MSamples - one for each channel. We will provide options of 240 MSamples/1 channel, 120 MSamples/2 channels and 60 Msamples/4 channels in the future once the application allows.
Two unit Linking	Two unit linking via Link In and Link Out Ports	The current design supports the existing Link Port - Link Port connection used by the CS328A without clock sharing. The next hardware iteration supports the HDMI cable based link port using Link IN- Link Out, and supports sample clock sharing. The hardware is currently being manufactured. We have taken the opportunity to add extra functionality to the second generation of hardware such as a self calibration voltage source and a high performance probe compensation source. We expect completed, second generation systems will be available in Oct 2018.
Signal Generator Waveforms	The signal generator will support AWB	The isolated Signal Generator currently only supports Sine wave generation and sweeping. The hardware (based on the AD9102) can generate 4K Arbitrary Waveforms, and patterns. The sig gen design includes a swept clock source to allow sweeping arbitrary waveforms (including square and triangle waves). The user interface for this is not yet done. We expect it to be done by Nov 2018.
Link Port	The Link includes SPI, UART and I2C generation	The Link Port includes the facilities to generate I2C, Uart and SPI messages, as well as digital outputs. This capability is already supported by the firmware and DLL driver. However a UI has not been implemented in the application. This will be done as time permits.
Real time Sample Filtering	Real Time sample filters to improve dynamic range	The filter block for the programmable FIR filter has been implemented, but is operating with a fixed coefficient set. The firmware to load a variable coefficient set still need to be implemented. This should be done by Oct 2018
Faster Peak Capture	Replay Peak Capture to run at close to real time	The current system has real time peak capture where the decimator outputs samples at below the maximum sample rate (eg Streaming). However, the replay peak capture system, while working, is not optimized and relatively slow. A DMA/Hardware based system will be used for peak capture replay. This should be done by Oct 2018.
Digital Port	Full use of Silego SLG46533V	Hardware has been tested. The UI has not been started. We will find a way to easily transfer designs to the Digital Port device sourced from the Silego Development tool.

Where a feature has not been implemented yet, it includes an asterisk in the table above.

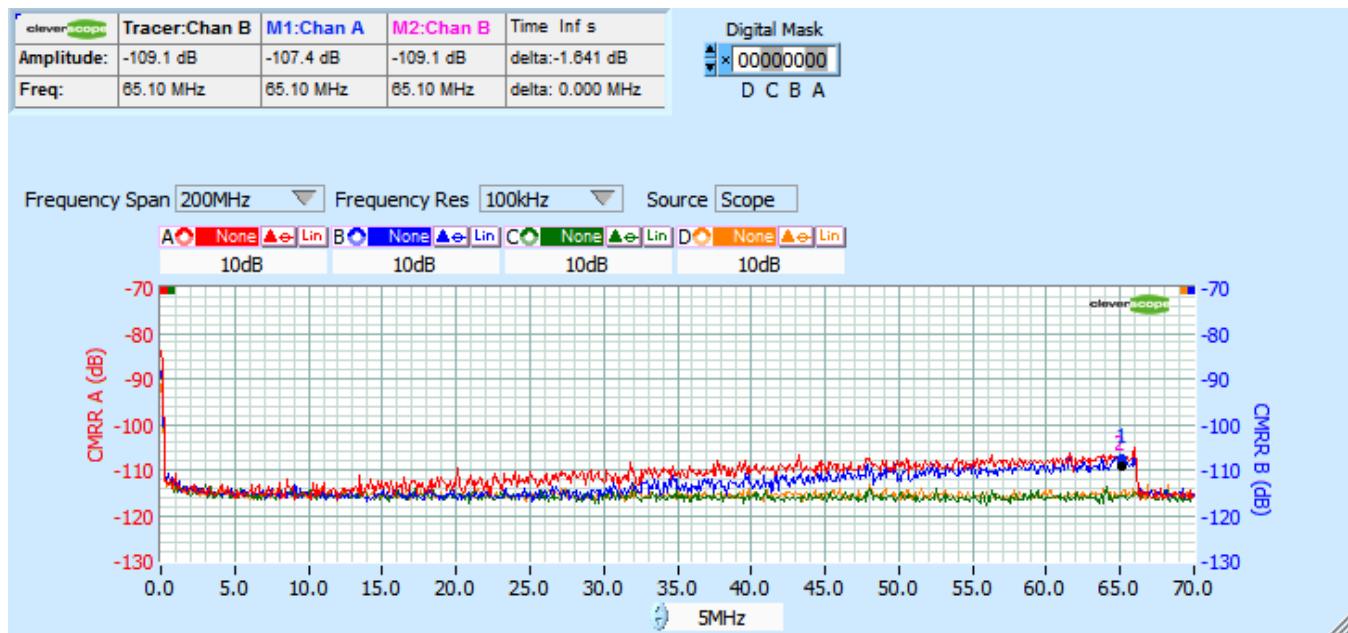
Selected Measurements

In this section we show some of the measurements that define the unique aspects of the CS448.

Common Mode Rejection

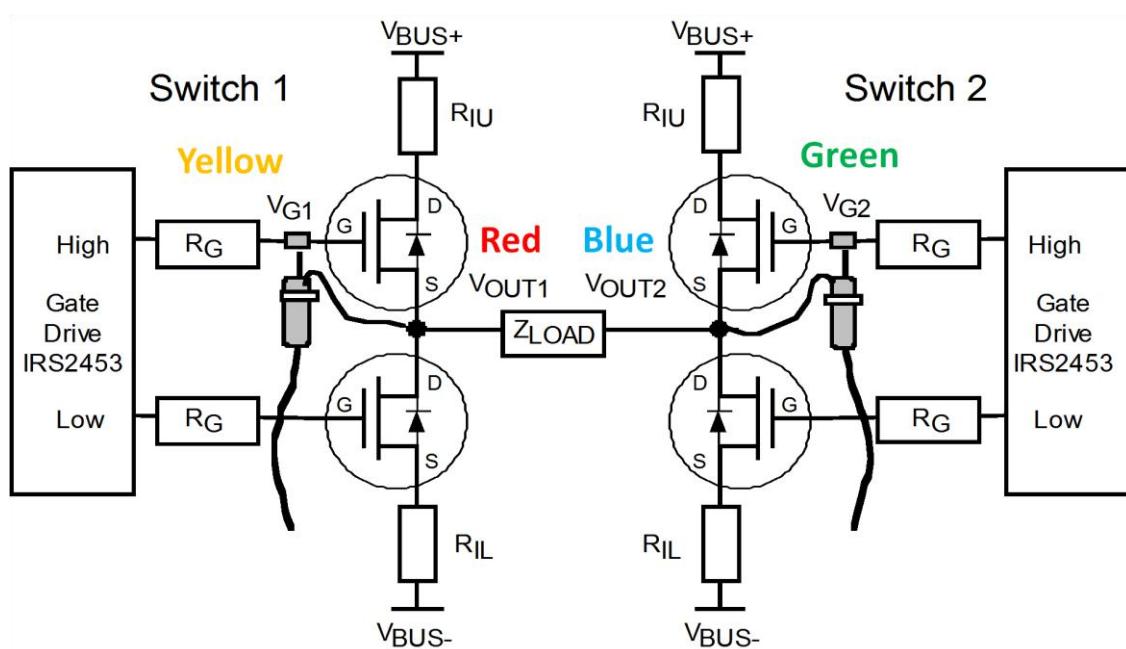
Channel A is being tested for CMRR using a 20 dBV source, and ranges from -120dB to -107dB. The scale is in dB CMRR.

Chans B,C and D show the dBV response to the Chan A common mode signal, and the response is in dBV. As the excitation used is +20 dBV, the leak through is about -125 dBc.

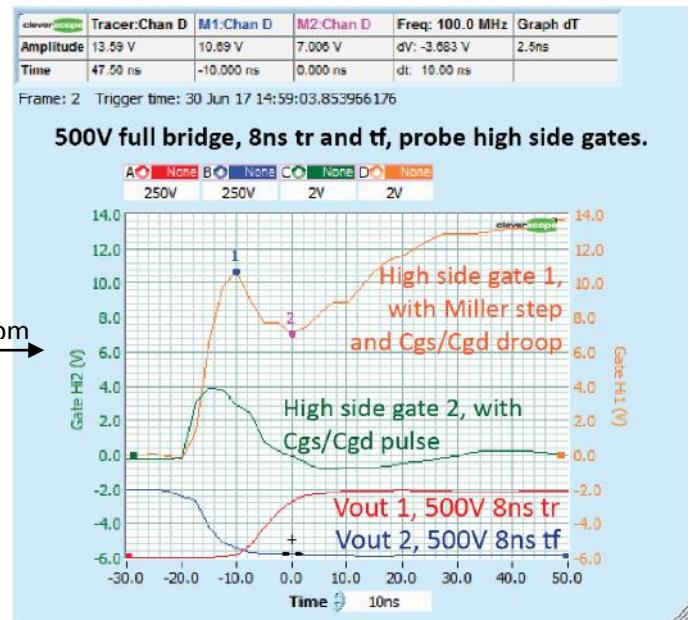
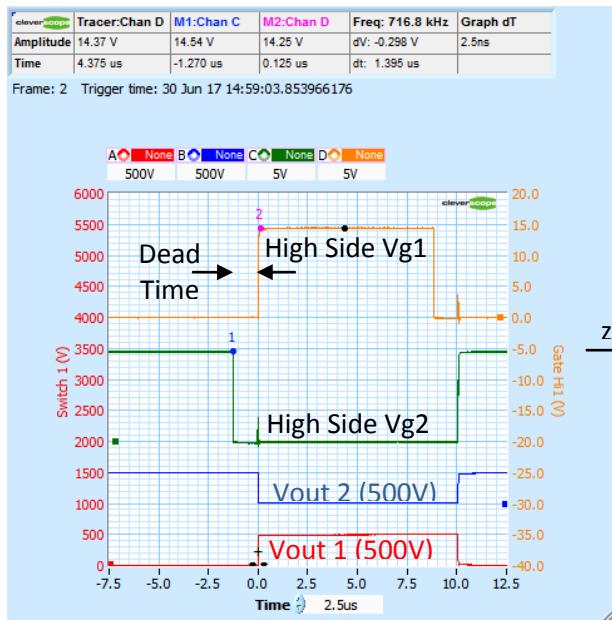


Application in switching Power Bridge

Using this full bridge setup, which swings 500V in 8ns:



We measure these results:

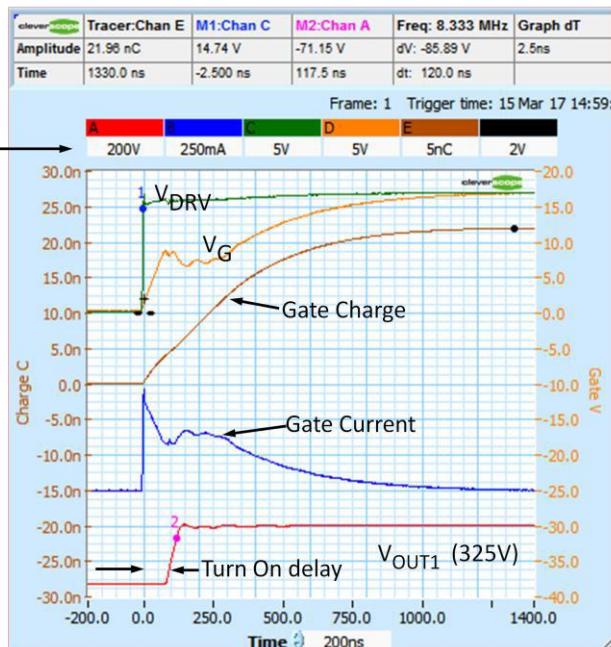
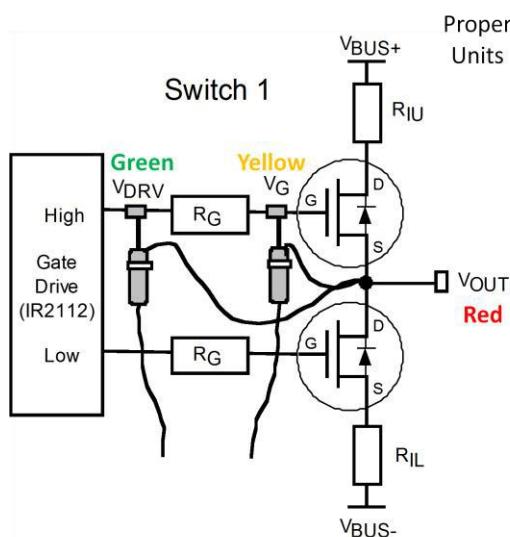


The high CMRR, and the isolation allow the high side gate drives to be measured without large common mode artifacts. We can observe dead time, pulse timing, the gate charge characteristic, and parasitics such as the Cgs/Cgd droop and pulse effects.

Measuring Gate Charge in a SEW Movitrac Variable Speed Drive (VSD)

Measuring Gate Drive System

Example: SEW Movitrac



Calculate Charge

$$Qg = \int Ig dt$$

Total Gate Charge

$$Qg = 22nC$$

Calculate Current

$$Ig = \frac{Vg - V_{DRV}}{RG}$$

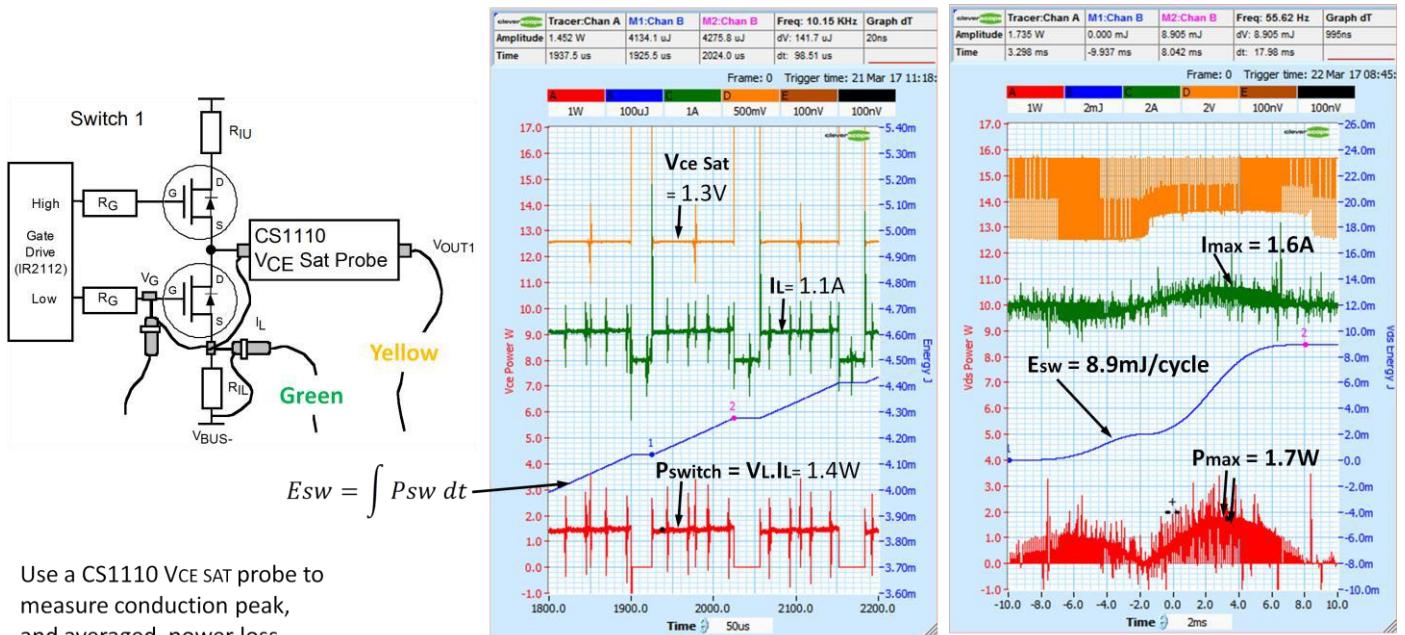
Plateau gate current

$$Ig = 400mA$$

The high CMRR, and isolation allow making differential measurements across the gate drive resistor, even though it is swinging 325V in 37ns. Maths is used to calculate the gate current which is then integrated to calculate charge.

Measuring Conduction loss in a SEW Movitrac VSD

We use a Cleverscope V_{CE} Sat probe to accurately measure small voltages while exposed to large (<1000V) voltage swings.

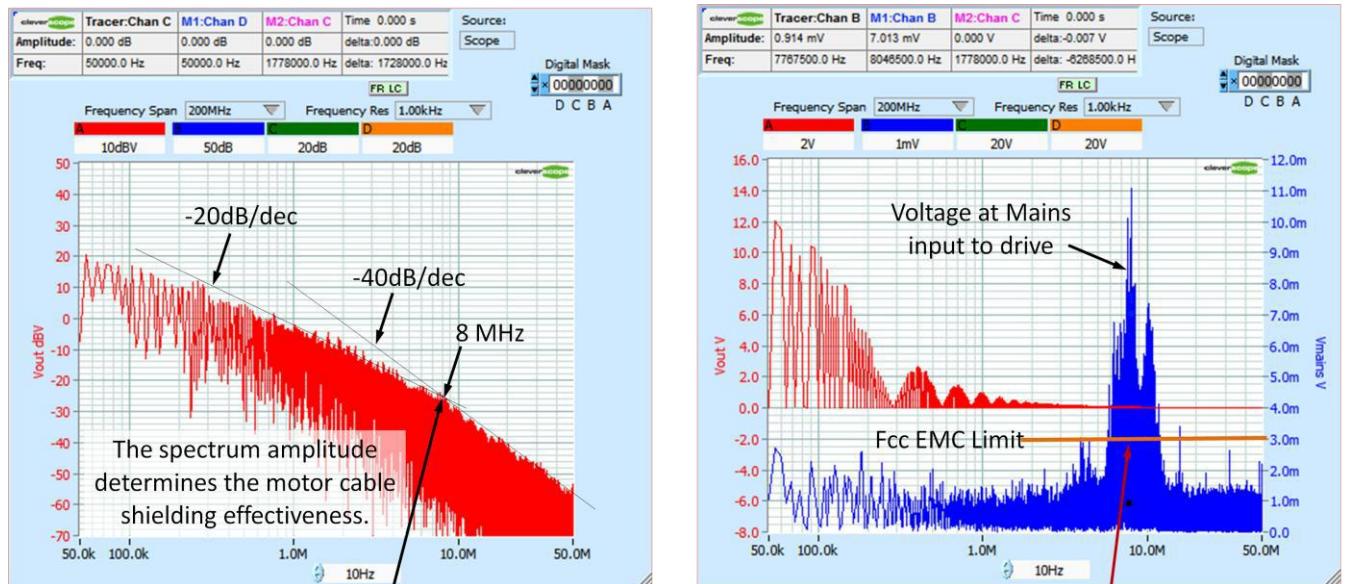


Use a CS1110 VCE SAT probe to measure conduction peak, and averaged power loss.

We use Maths to calculate the conduction current (green), the V_{CE} Sat probe to measure the switch saturation voltage (Yellow), the instantaneous power (red) and the energy per cycle (blue) to calculate the average conduction loss power (494 mW).

Measuring required shielding performance and EMC filtering effectiveness

We use 100x probes to measure the Switch voltage, and the input mains voltage safely.



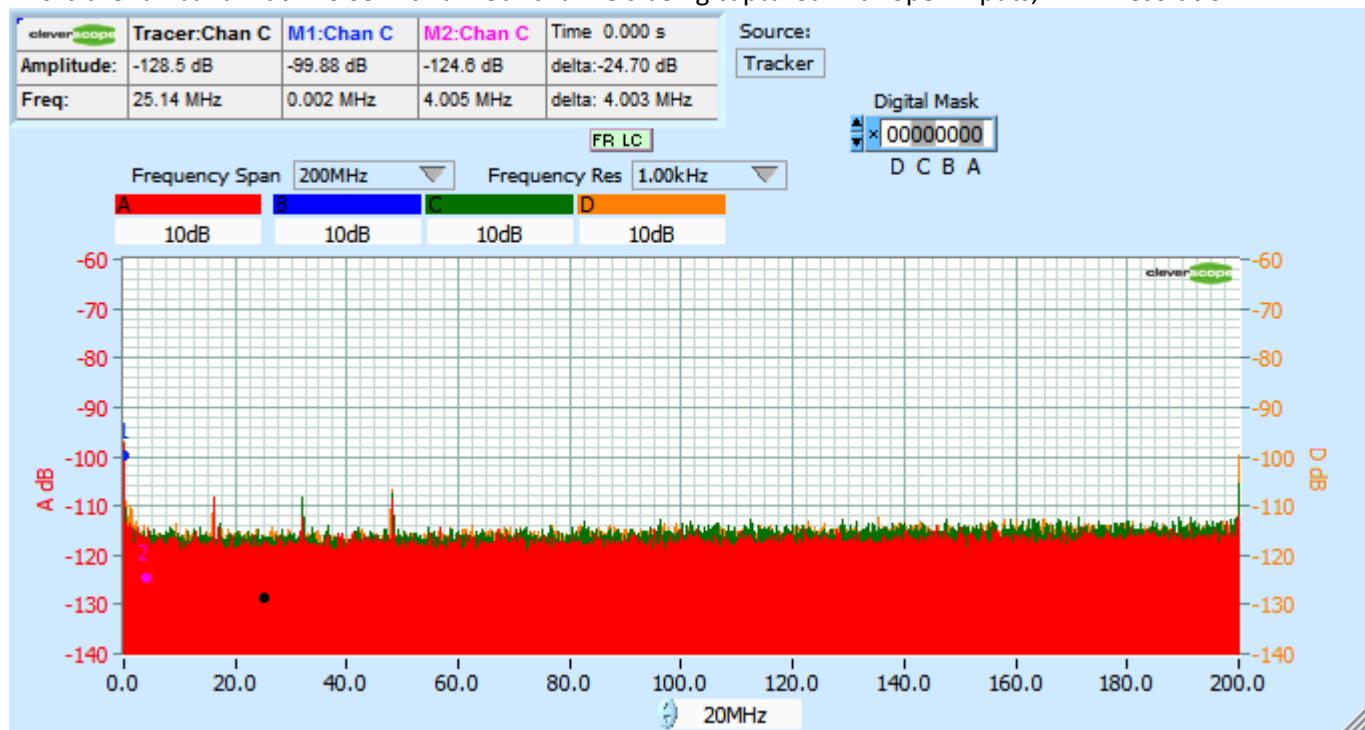
The 20/40 dB/dec corner frequency is set by the rise time ($F = 1/\pi 37\text{ns}$). A slower rise time reduces how good the shield needs to be.

The mains input is not sufficiently filtered, and the drive does not meet the FCC standard. A slower rise time would help, and improved filtering.

This test uses the Spectrum Analyser.

Spectral Noise Floor

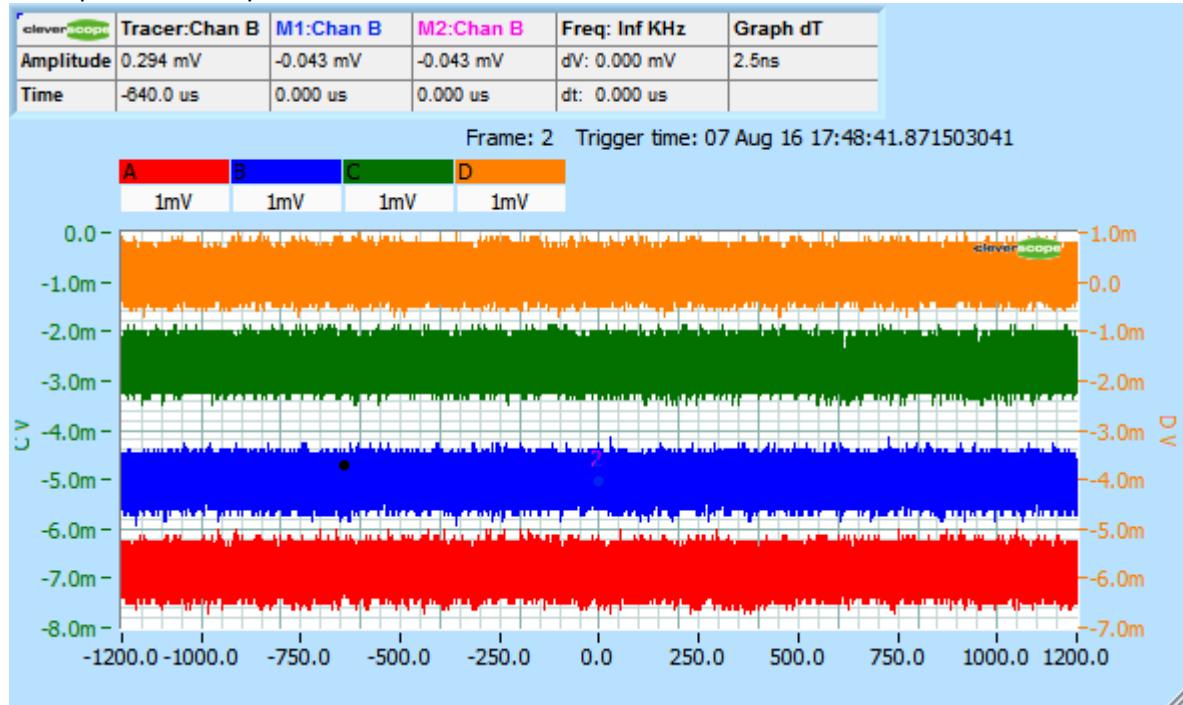
This is the full bandwidth noise with all four channels being captured with open inputs, 1kHz resolution:



The three peaks are related to the front end processor 8 MHz clock. We will be working on reducing these.

Time Noise Floor

We capture 1M samples:



We use the signal information display to calculate the Standard Deviation (a good estimate of RMS, less the DC) and the peak to peak. We see less than 200uVrms noise, and less than 1.8mV p-p noise.

The signal information for $\pm 0.8V$ is:

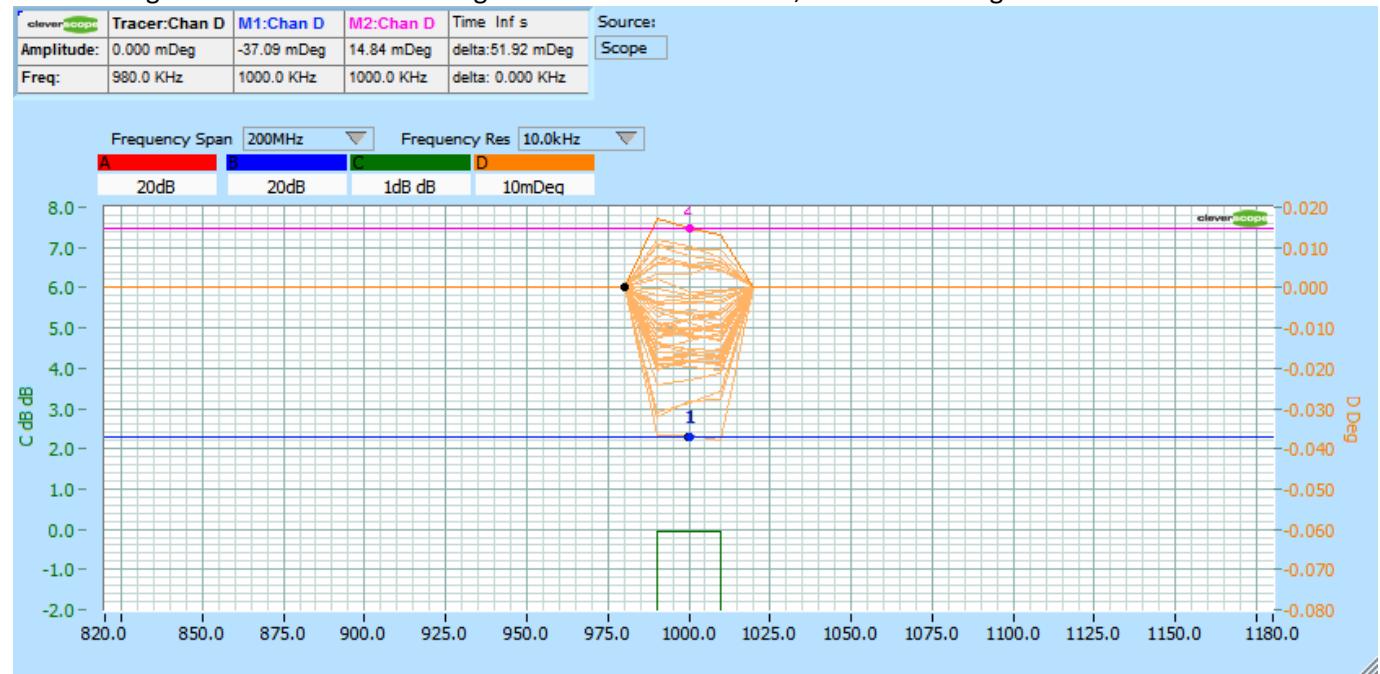
Signal Information					Show Logging
Function	Chan A	Chan B	Chan C	Chan D	
DC	-1.860 mV	-17.38 uV	-2.691 mV	161.2 uV	
RMS	1.870 mV	188.5 uV	2.698 mV	253.7 uV	
Max	-1.028 mV	856.1 uV	-1.876 mV	1.014 mV	
Min	-2.731 mV	-942.7 uV	-3.494 mV	-719.6 uV	
Pk-Pk	1.703 mV	1.799 mV	1.618 mV	1.734 mV	
Std Dev	192.9 uV	187.9 uV	202.1 uV	196.4 uV	
Period	23.75 ns	10.83 ns	15.42 ns	35.00 ns	
Fundamental Frequency	2.734 kHz	240.1 kHz	5.660 kHz	27.18 kHz	
Fundamental Peak amp	17.13 uV	33.57 uV	14.12 uV	17.94 uV	
Pulse Length	10.83 ns	6.183 ns	6.364 ns	9.896 ns	
Duty Cycle	54.21 %	55.77 %	75.68 %	37.50 %	

The signal information for $\pm 8V$ is:

Signal Information					Show Logging
Function	Chan A	Chan B	Chan C	Chan D	
DC	-17.94 mV	-8.874 mV	-24.97 mV	-209.5 uV	
RMS	18.07 mV	9.086 mV	25.04 mV	1.946 mV	
Max	-11.00 mV	-1.980 mV	-16.64 mV	7.044 mV	
Min	-24.54 mV	-16.64 mV	-33.56 mV	-7.620 mV	
Pk-Pk	13.54 mV	14.66 mV	16.92 mV	14.66 mV	
Std Dev	1.939 mV	1.956 mV	2.006 mV	1.934 mV	
Period	2.640 us	5.280 us	2.920 us	930.0 ns	
Fundamental Frequency	3.992 kHz	463.2 kHz	1.618 MHz	2.249 kHz	
Fundamental Peak amp	215.0 uV	142.4 uV	172.9 uV	201.7 uV	
Pulse Length	681.4 ns	1.157 us	1.241 us	896.4 ns	
Duty Cycle	13.64 %	45.45 %	89.05 %	29.03 %	

Channel to Channel Skew

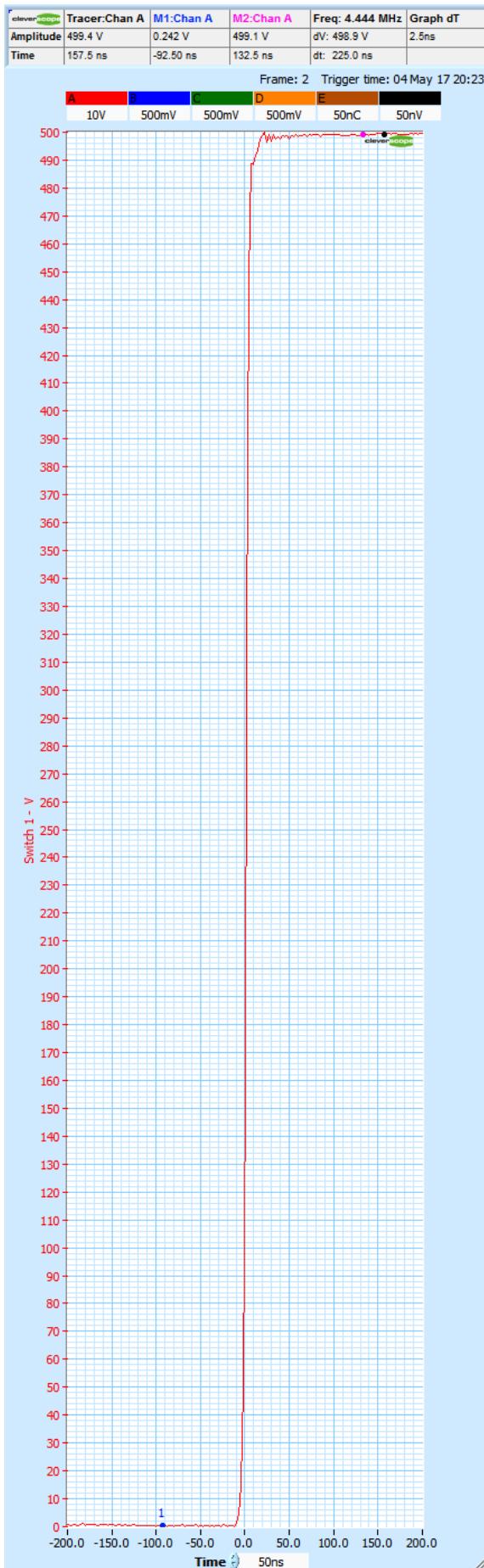
Channel to Channel Skew should be low to allow Frequency Response Analysis. Using two channels driven by the same Signal Generator and two length matched coaxial cables, with a 1 MHz signal we measure:



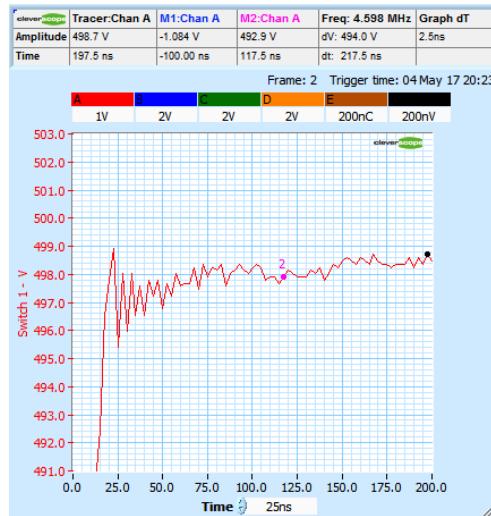
Persistence has been turned on to show the variability. We use Gain/Phase to make the measurement between Chans C and D. Gain was 0 dB. The phase varied from -0.037 deg to + 0.015 deg, a variation of 0.052 deg at 1 MHz. This is the same as $0.052/360 \times 1\mu s = 144$ ps p-p variation. This is the same as 1 degree at 19.2 MHz.

Response to 500V 10ns transition

We measure the CS1090 Switch 1 output (500V, 10ns rise time):



This trace shows the transition measured using a 100x probe. The display pixel resolution masks the actual channel resolution, shown here at 1V/div:

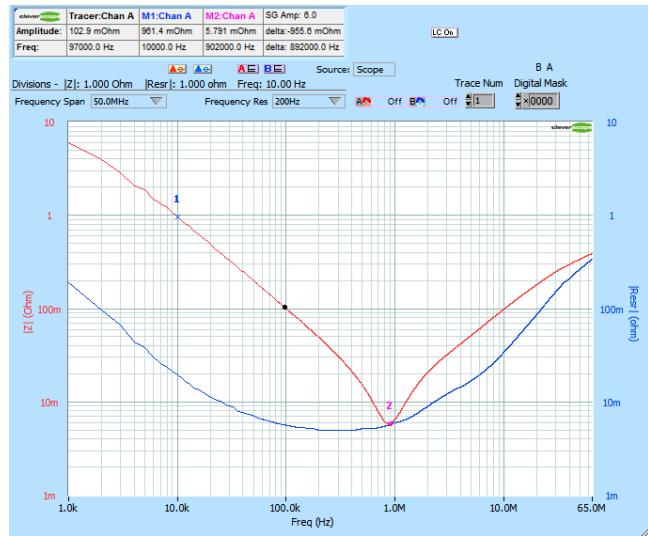


This kind of resolution is not possible with an 8 bit scope.

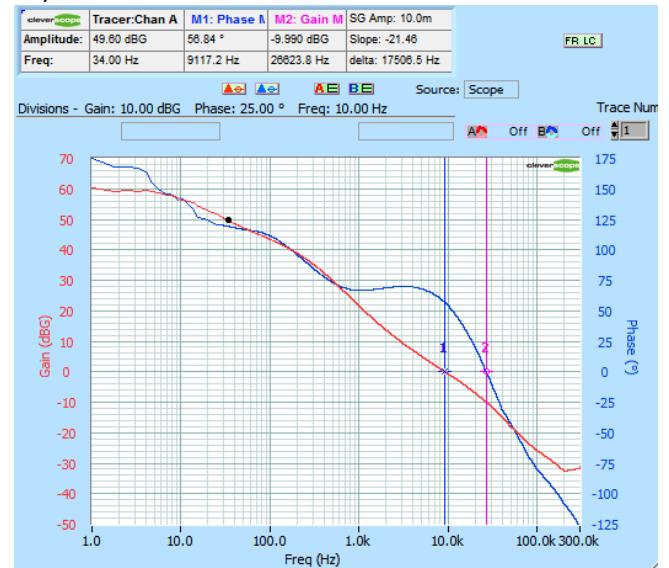
Frequency Response Analysis Functions (FRA)

The Frequency Response Analysis (FRA) system uses the isolated signal generator to provide stimulus for component, system or power supply measurements. The measurements available are shown in the Displays/FRA section of the data sheet. Here are a collection of measurements made using the FRA system (zoom on the PDF to see the detail):

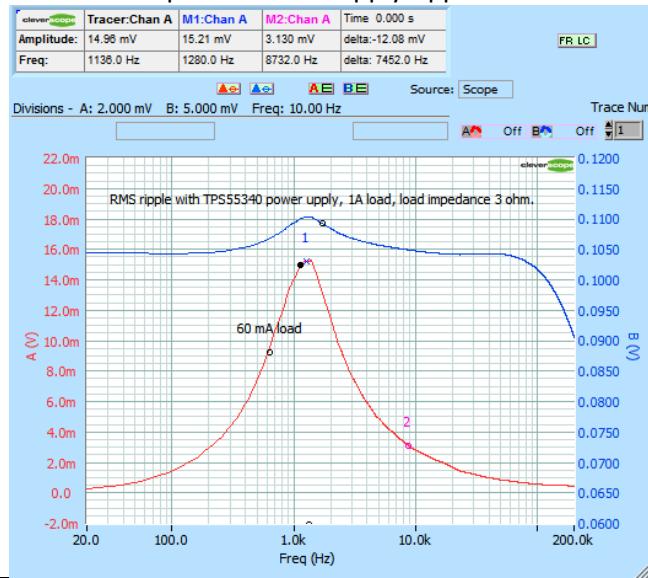
Impedance of a ceramic capacitor



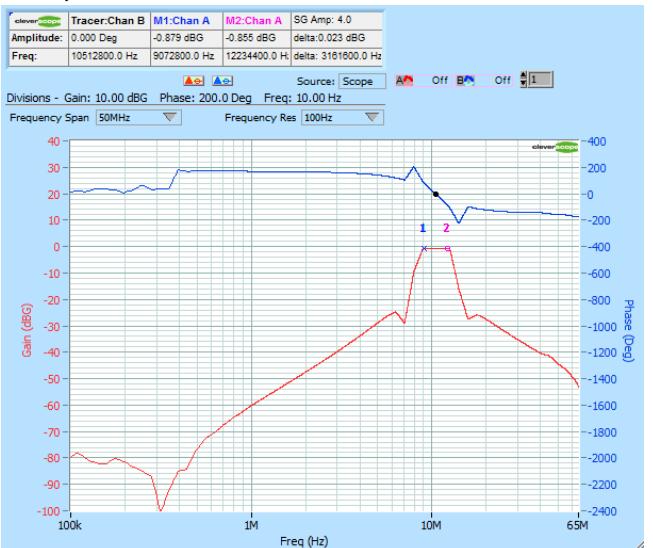
PSU Gain Phase of switching power supply TPS55340 showing Phase Margin (56.8 deg) and Gain Margin (20 dB):



PSU Shunt Impedance and supply ripple TPS55340:



Gain/Phase of a 10.7 MHz filter:



TLV70433 PSRR using CS1070 (1A 50 MHz op-amp):



Powered LTC3589 Output Impedance using CS1070:



Cleverscope Application Specification

Calibration

Calibration method	Automatic self calibration
Calibration Voltage Source	2.5V reference, $\pm 0.15\%$ accuracy, 30 ppm/deg C

Displays

Windows	Simultaneous Capture, Tracking, Spectrum, Information, Maths, XY, Control Panel, Streaming, Frequency Response Analysis (FRA) and Protocol setup windows
Scope window functions	Defines capture specification for signal acquisition unit, defining amount of time before trigger, amount of time after the trigger, lower amplitude limit, upper amplitude limit. Defines Tracking graph time position, when tracking graph is linked. Defines trigger level and direction Full zoom and Pan in both axis. Annotations. Custom units Custom colours
Tracking window functions	Displays zoomed section of captured signal. Resolution from 1ns to 5s/div. Full zoom and Pan in both axis. Annotations. Custom colours
Spectrum window functions	Display spectrum of signal captured in capture window. User definable resolution Full zoom and Pan in both axis. Annotations. Custom units Custom colours
Maths window function	Displays results of Maths equations. Maths equations are user entered expressions involving any of the inputs (analog and digital), previous maths equation line results, and an arbitrary number of function results (+ - * / sqrt, power, log, ln, all transcendental functions, equality functions). Custom units. Provide live Matlab link.
XY window function	Displays XY graph from source (Capture, tracking, spectrum, or Maths)
Information window functions	Displays automated measurements (see below) Used to log derived information values to disk, with a period of between 0.05 – 86,400 secs per sample. Live logging to Excel DDE live value transfer to Excel.
Control window functions	Provides Trigger settings – analog and digital Provides Sample control – single, triggered or automatic. Provides access to tools – Pan, Zoom, Annotate Controls Frame store Controls Spectrum resolution, acquisition method and averaging
Frequency Response Analysis (FRA)	FRA control panel is used to setup up oscilloscope/signal generator to make automated measurements of these values vs frequency: <ul style="list-style-type: none"> • RMS Amplitude • Power • Power Density • Gain/Phase • Impedance + R_{ESR} or Q/D Factor or Phase • Capacitance + R_{ESR} or D Factor or Phase • Inductance + R_{ESR} or Q Factor or Phase • Shunt Impedance (magnitude without phase for low impedances) • PSU Gain/Phase - for finding Gain/Phase of powered up power supplies • PSU PSRR - for finding PSRR of powered up power supplies • PSU Output Impedance - for finding Output Impedance of powered up power supplies • PSU Input Impedance - for finding Input Impedance of powered up power supplies • Probe calibration functions for maximum accuracy.
Protocol Setup	Provides protocol setup for I2C, SPI, UART and parallel bus.

Measurements

Cursors	Voltage Difference between cursors Time difference between cursors Reciprocal of ΔT in Hertz ($1/\Delta T$).																																																																																
Automated measurements	<table border="1"> <tr><th>Function</th><th>Function</th><th>Function</th><th>Function</th><th>Function</th></tr> <tr><td>DC</td><td>0 -> 1 Time</td><td>DC</td><td>A at F</td><td></td></tr> <tr><td>RMS</td><td>1 -> 0 Time</td><td>RMS</td><td>B at F</td><td></td></tr> <tr><td>Max</td><td>V '1'</td><td>Fsignal</td><td>A max</td><td></td></tr> <tr><td>Min</td><td>V '0'</td><td>Vsignal</td><td>A min</td><td></td></tr> <tr><td>Pk-Pk</td><td>V swing</td><td>F1</td><td>B max</td><td></td></tr> <tr><td>Std Dev</td><td>Overshoot</td><td>V1</td><td>B min</td><td></td></tr> <tr><td>Period</td><td>Slew rate</td><td>F2</td><td>Amax at 0 B</td><td></td></tr> <tr><td>Fundamental</td><td>Pulse</td><td>V2</td><td>Amin at 0 B</td><td></td></tr> <tr><td>Frequency</td><td>Period</td><td>F3</td><td>Bmax at 0 A</td><td></td></tr> <tr><td>Fundamental</td><td>Pulse</td><td>V3</td><td>Bmin at 0 A</td><td></td></tr> <tr><td>Peak amp</td><td>Frequency</td><td>SINAD</td><td>A -3dB L: H</td><td></td></tr> <tr><td>Pulse</td><td>Pulse</td><td>THD</td><td>B -3dB L: H</td><td></td></tr> <tr><td>Length</td><td>Length</td><td></td><td></td><td>HD2+3</td></tr> <tr><td>Duty Cycle</td><td>Duty Cycle</td><td></td><td></td><td></td><td></td></tr> </table>					Function	Function	Function	Function	Function	DC	0 -> 1 Time	DC	A at F		RMS	1 -> 0 Time	RMS	B at F		Max	V '1'	Fsignal	A max		Min	V '0'	Vsignal	A min		Pk-Pk	V swing	F1	B max		Std Dev	Overshoot	V1	B min		Period	Slew rate	F2	Amax at 0 B		Fundamental	Pulse	V2	Amin at 0 B		Frequency	Period	F3	Bmax at 0 A		Fundamental	Pulse	V3	Bmin at 0 A		Peak amp	Frequency	SINAD	A -3dB L: H		Pulse	Pulse	THD	B -3dB L: H		Length	Length			HD2+3	Duty Cycle	Duty Cycle				
Function	Function	Function	Function	Function																																																																													
DC	0 -> 1 Time	DC	A at F																																																																														
RMS	1 -> 0 Time	RMS	B at F																																																																														
Max	V '1'	Fsignal	A max																																																																														
Min	V '0'	Vsignal	A min																																																																														
Pk-Pk	V swing	F1	B max																																																																														
Std Dev	Overshoot	V1	B min																																																																														
Period	Slew rate	F2	Amax at 0 B																																																																														
Fundamental	Pulse	V2	Amin at 0 B																																																																														
Frequency	Period	F3	Bmax at 0 A																																																																														
Fundamental	Pulse	V3	Bmin at 0 A																																																																														
Peak amp	Frequency	SINAD	A -3dB L: H																																																																														
Pulse	Pulse	THD	B -3dB L: H																																																																														
Length	Length			HD2+3																																																																													
Duty Cycle	Duty Cycle																																																																																
Custom units	6 characters																																																																																
Custom signal names	20 characters																																																																																
Custom scaling	Scale + offset by defining two (Vin,Vout) points																																																																																
User definable colours	Signals, Background, Major Grid, Minor Grid																																																																																

Mathematical Functions

Functions over the signal	Differentiation, Integration, Filtering, Power functions, Matlab interface, Signal Processing functions
Functions on a data point	Addition, subtraction, multiplication, division, squaring, square root, (inverse) sine, cosine, tangent, tangent, log, sign etc. Equality operations.
Maximum number of sequential mathematical equations	10, symbolic with multiple operators and operands.

Spectrum Analysis

Frequency Range	User definable, Range = 0- 1/Scope Graph ΔT Frequency axis – log or linear.
Analysis Output	RMS Amplitude, Power, Power Density, Gain/Phase
Frequency Resolution	In 1, 2, 2.5, 5 sequence with 1 part in 1M resolution.
Output type	Volts, Power, Gain/Phase in linear , dB, degree or radian values. Impedance, LCR, Q and DF. Custom units can be applied.
Window types	None, Hanning, Hamming, Blackman-Harris, Flat top, Low Sidelobe
Averaging	Moving average, block average, peak hold.
Averaging method	Vector averaging in time domain if triggered. RMS averaging in frequency domain if not triggered.

Protocol Decode

Protocols	I2C, SPI , UART and parallel bus.
Protocol decode inputs	Digital Inputs 1-8, External trigger, Channels A, B User defined threshold when using analog inputs
Protocol decode variables	Number of bits, Clock edge rising or falling, Bit invert/non Invert, Select Hi/Lo, MSB first or not, Number of stop bits.
Output display type	Naming label. Character, Hexadecimal or Decimal Number. Colour.

Streaming

Sampling Rate	1 SPS – 3 MSPS (USB2) or 30 MSPS (USB3)
Sample preparation	Peak capture or Moving average filter prior to decimation. Using 1.28us filter with 12 or 14 bit ADC we achieve 16 bits ENOB at 1 MSPS.
Sample storage	Up to 500 G samples. Samples are stored in multiple smaller files to increase speed.
Review capabilities	Zoom and pan anywhere in sample space. Samples are displayed peak captured (ie 1us pulse will still be visible in 1 day long sample record).
Export capabilities	Export tab delimited text, binary, or cleverscope format file. Output between markers, or current display. Set output depth.

Data Export

File types output	Cleverscope proprietary, Tab delimited text (Excel compatible), Excel file (for signal information logging).
Live Data output	DDE to Excel, direct placement of data into live Excel sheet Live data output to and return from Matlab

Windows facilities

Standard Functions	Copy and Paste Save and Open native format (saves full setup) Save and Open tab delimited text file Save and Open binary file (start time, dt, data) Print with Date/Time, File Name and Description. Print Setup
Windows	Dynamically resized Can be placed anywhere on desktop Can be docked to move with Control Panel Can be docked to minimize/restore with one click.
User defined units	6 characters
User defined signal names	20 characters
User defined scaling	Scale + offset by defining two (Vin,Vout) points
User definable colours	Signals, Background, Major Grid, Minor Grid

Document changes:

5 May 2017 v1.1 - Original
 12 July 2018 v1.2 - Added Specification Status section.