American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

By: Michael Creeden, CID+ Insulectro, Technical Director Design Education
January 2022

Solve Micro Pitched BGA & High Density Circuits Reliably with Ormet® Z-Axis Interconnects

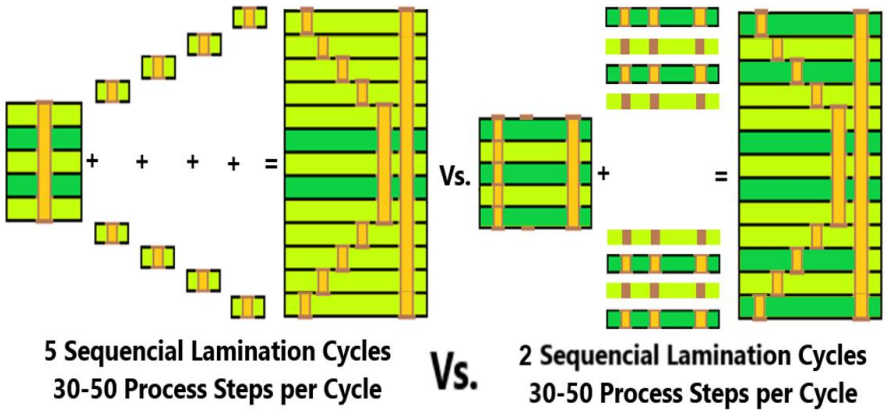
Often people are afraid to use a technology they're not familiar with, so my hope is to familiarize you with a solution called, **"Ormet® Z-Axis Interconnects"** that **American Standard Circuits** is eager to help you utilize. This product has experienced industry acceptance for over a decade and today's circuit challenges are requiring innovation to meet these challenges. Today's designs are pushing the barriers on several fronts simultaneously, such as: High-speed circuitry that must meet signal integrity concerns, advanced packaging with µBGA pin pitch requiring (HDI) High Density Interconnect solutions, along with advanced drilling requirements that can't be solved with traditional manufacturing process, such as, back to back buried vias. **Ormet® Z-Axis Interconnects** meets these challenges head-on. You'll see it does so reliably with a cost effective approach.

Ormet® Z-Axis Interconnects are created with a material and process that conductively paste fills a via on any layer, rather than plating the via wall for Z-Axis connectivity. The paste material is an alloy formed from Copper and Tin/Bismuth and the process is called, "(TLPS) Transient Liquid Phase Sintering." In this article, we are not going to inform you on how the fabricators implement this solution, rather, we wish to explain how you can solve your circuit challenges by utilizing **Ormet® Z-Axis Interconnects**.

The overview of design challenges we will cover are as follows:

- Reduced Lamination Cycles - Saving time & money
- Any-Layer-Vias HDI = Design freedom
- Eliminate High-Aspect-Vias, used on high layer count boards
- Eliminate Back-Drilling, no stubs on high-speed signals
- Increase routing resources

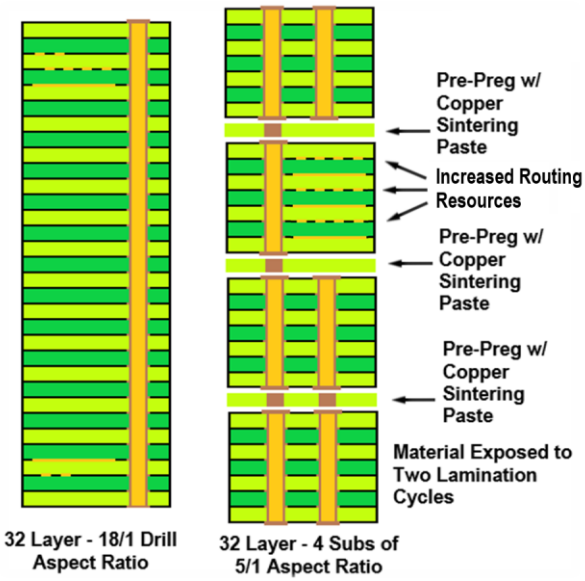
In today's circuits, µBGAs with a pin-pitch of .65mm or below requires the implementation of HDI. This is no longer a choice but a requirement. The standard method to fabricate these boards is using laser drilled µVias and sequential lamination, whereby a core set of layers typically will have many process steps in a build-up fashion: Adding layers with lamination cycles, drill, etch and plate. Many common HDI builds require 3-5 lamination cycles. Each lamination cycle can consist of approximately 30-50 process steps. Each one of these process steps can add a significant number of days to the fabrication build, with the sum total ranging from 3-5 weeks. All of this adds cost, schedule delays, and threatens long term reliability as the board re-enters a thermal excursion from the lamination heat press multiple times.



Reduced Lamination Cycles - Saving Time & Money

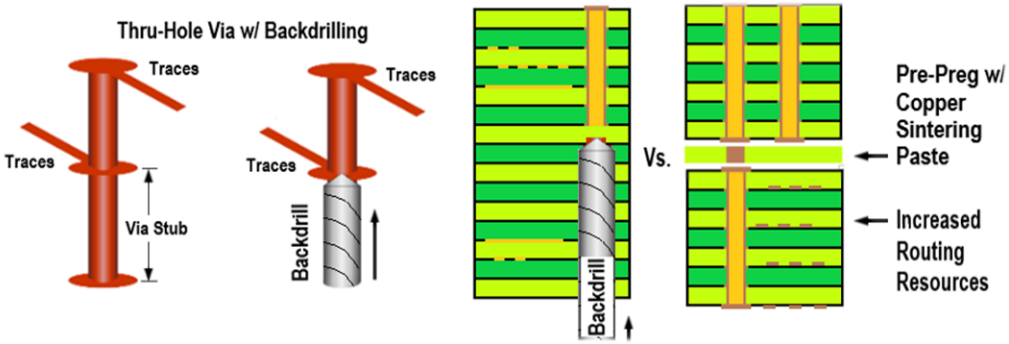
The left image illustrates the conventional method requiring 5 lamination cycles and the right image illustrates the same board completed in half the time with 2 lamination cycles using **Ormet® TLPS.** This allows the

fabricator to apply via paste to add the outer layers and accomplish the same construction with a total of 2 lamination press cycles with approximately a 150 fewer process steps. This can result in faster build time at lower costs.



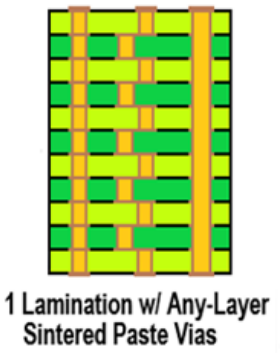
Elimination of High Aspect Ratio Vias on High Layer Count Boards

High layer count boards with small drill sizes result in drill/plate aspect ratios that are extremely difficult to build with any reliability. In the **Ormet® TLPS** example on the right side, we would build 4 sub-lam constructions and then join them together with **Ormet®** paste inside of three pre-preg layers. This transforms an 18/1 aspect ratio drill into four 5/1 aspect ratio drills. The side benefit is you can use the vias only where it is needed, thus creating significant routing resources, and improving signal integrity as well.

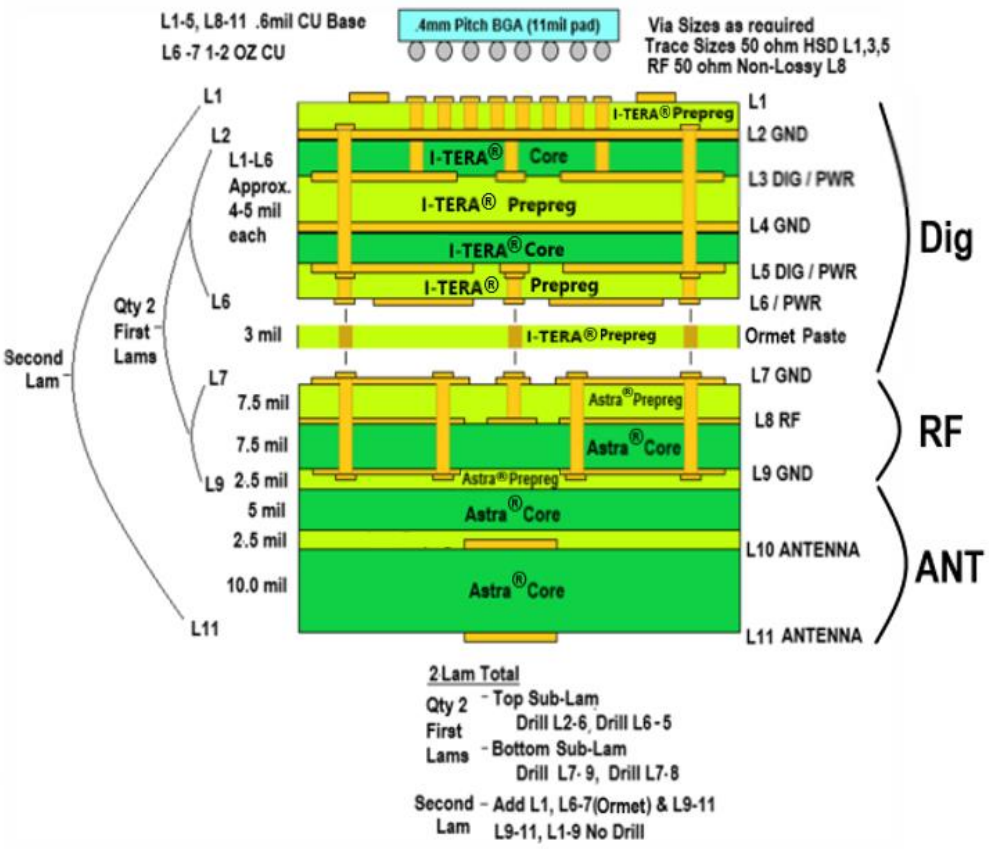


High-speed Signals with No Backdrilling

Ormet® TLPS eliminates controlled-depth backdrilling requirements for high-speed signals, thus eliminating parasitic stubs, also significantly increasing routing resources that backdrilling prohibits. Backdrilling has always been a risky design concern and a field reliability concern.



Ormet® TLPS – Any Layer Via usage has been used extensively in the Package Design sector of electronics since its inception. This is the transposer board that is used on most BGA packages. The die (Chip-on-board) routes vertically to the BGA balls on the bottom side of this BGA interposer board. These interposer boards often will have many layers with very thin dielectric thicknesses. This Any Layer Via usage on thin boards is the only method to route Package Designs.



5G Next Generation Innovation for HSD-RF Hybrid Technology

Ormet® TLPS can be the only solution to solve some of the newer challenges of HSD-RF Hybrid technology boards as used in the 5G world. The complexity of hybrid circuits that combine fine pitch µBGAs along with circuit requirements of High Speed Digital, RF, Printed Antennas, and significant thermal concerns can only be met with this form of HDI. This is compounded by the fact that boards with antennas often make for a fabrication nightmare based on their unbalanced construction and uneven layer counts.

Discuss these ideas early with your fabricators' engineering team. We're encouraging you to evolve your thinking from, *"Design For Manufacturing,"* to, ***"Design With your Manufacturer!"***